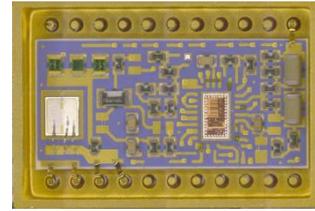


35W DC/DC Converter Controllers



FEATURES

- Wide input power bus range: 19V to 60V and 50V to 105V within derating rules ECSS-Q-ST30-11C
- Integrated start-up circuitry
- Integrated power switch
- 100kHz to 1MHz switching frequency
- Synchronization capability to external clock
- Output over-power protection
- Under-voltage protection
- Over-voltage protection
- ON-OFF capability
- Operating temperature range -35°C to 90°C within derating rules ECSS-Q-ST30-11C
- Radiation tolerant: TID 100krad, SEL 60 MeV·cm²/mg
- Export restriction free

APPLICATIONS

- Isolated Multi output DC/DC converters
- Non-isolated Multi output DC/DC converters
- Flyback topology
- Forward topology
- DC/DC Power output up to 35W
- Satellite systems
- Launch vehicles

DESCRIPTION

The DC/DC converter controller series simplifies the design of isolated and non-isolated DC/DC converters which are based on a primary low-side power transistor (e.g. flyback topology). The XXHFC100 can directly interface the input power bus in a wide voltage range, 50V-105V, without need of additional components, while the XXHFC60 which optimize the efficiency for lower input voltages is capable to directly interface bus voltages in the range 19V-60V.

The design effort of single and multi-output DC/DC converters will be reduced to designing the main transformer, the output rectifier stage and input and output filters while all the other functionalities, including over-current, under-voltage, over-voltage and over-temperature protection are implemented within the DC/DC converter controller.

The switching frequency of the converter is settable from 100kHz to 1MHz with an external resistor. Lead edge blanking and maximum duty cycle are set as minimum on-time ($t_{ON,MIN}$) and minimum off-time ($t_{OFF,MIN}$) internally. The maximum duty cycle is set to 50%, with the possibility to increase it by an adjustment resistor connected between ground and the DC_ADJ pin.

The slope compensation and the soft start are also set internally. A pulsed current is provided for magnetic feedback applications at pin MFB. Optical feedback provided by an optocoupler can be connected to the COMP pin. For non-isolated topologies the internal error amplifier is accessible via VFB.

The Arc Power DC/DC controller series is designed, manufactured and tested according to ECSS-Q-ST-30-11C and ECSS-ST-60-05C.

FUNCTIONAL BLOCK DIAGRAM

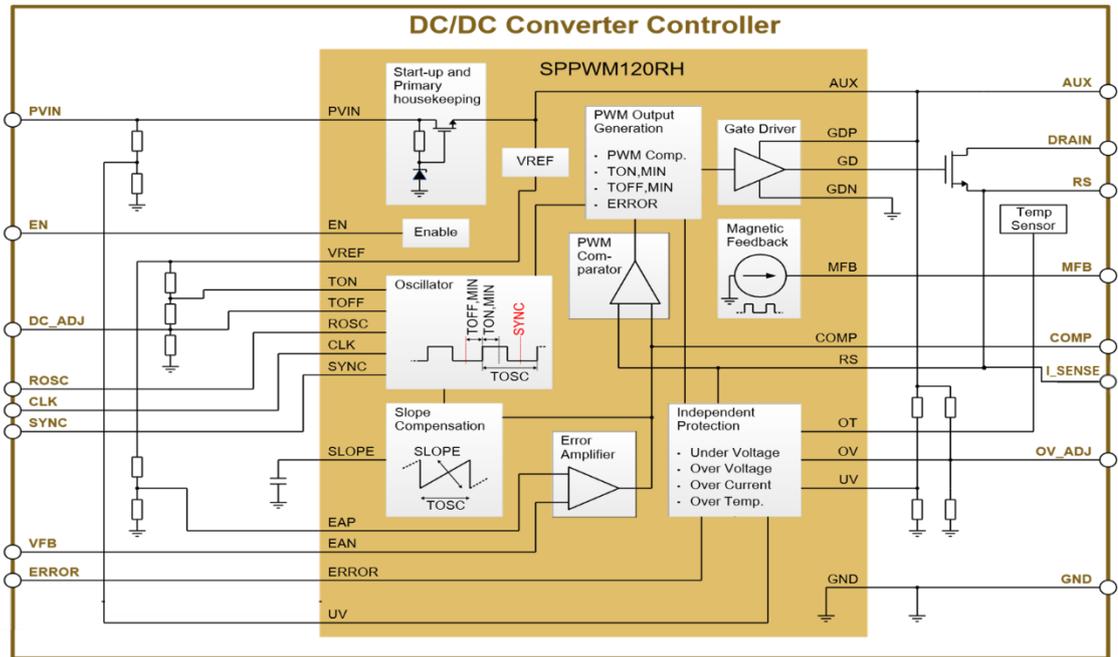


Figure 1: Block diagram

ISOLATED FLYBACK TOPOLOGY CONNECTION DIAGRAM

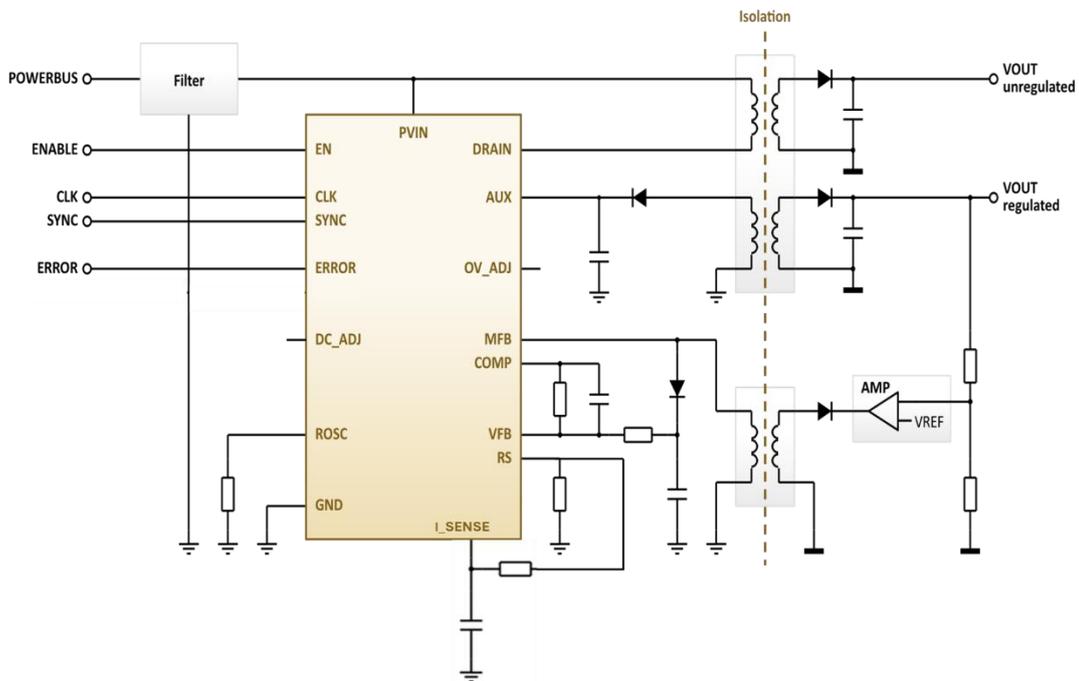


Figure 2: Isolated Flyback topology interconnection diagram

Mechanical and Electrical interfaces

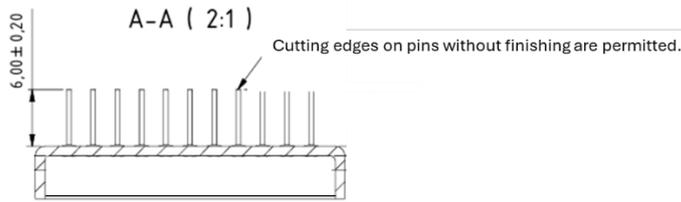
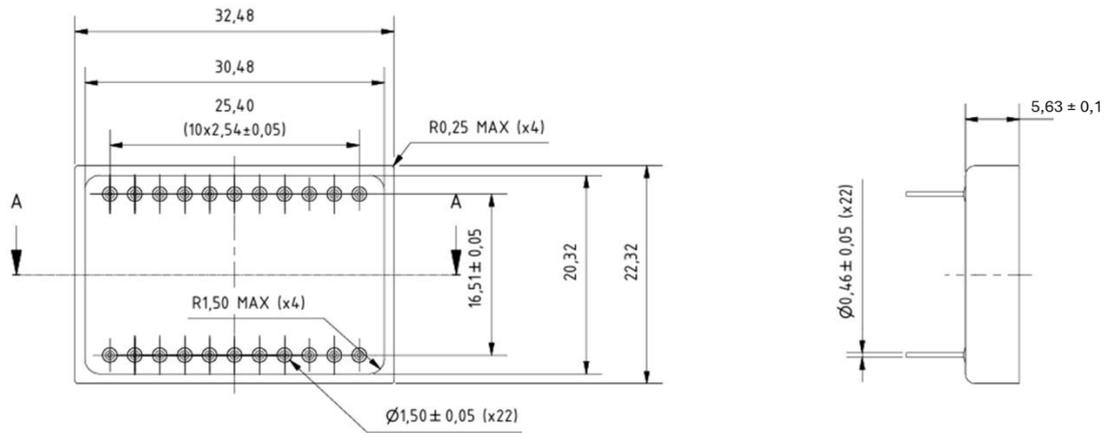
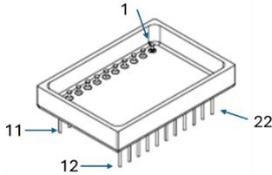


Figure 3: Mechanical drawings

Pin function

Top view:



Pin Name	Pin Number	Pin Description
DRAIN	1, 2	Low side power MOSFET drain to be connected to transformer primary winding.
RS	3,4	Source of the MOSFET to be connected to current sense resistor to obtain a voltage proportional to the switch current. This signal is used by the PWM to terminate the switch conduction.
PVIN	5	Power bus input to supply the device.
AUX	6	Voltage for the primary housekeeping and the gate driver supply.
OV_ADJ	7	Connection point for the adjustment resistor for fine tuning of the latching overvoltage threshold. This pin can be used as monitor signal for the auxiliary voltage value.
EN	8	Enable input pin: The EN pin is a digital input pin that enables or disables the regulator. Set the EN pin high to turn the regulator on; set it to GND, to turn the regulator off. An OFF/ON sequence will reset the latching protections.
ERROR*	9	Inverted error signal, open drain output. Will pull the pin to GND in case a critical error occurred.
I_SENSE	10	Input pin for the current sense signal; shall be connected to filtered signal present on Pin 3 and 4 of the hybrid. The operating voltage shall be <1V; if the 1V limit is reached the controller will limit the duty cycle triggering the output over-power protection.
NC	11	Not connected pins; shall be grounded to a reference voltage.
GND	12	Power bus return, ground reference.
MFB	13	Magnetic feedback: Pulsed current will be applied to this pin to transfer the feedback from the secondary side via an external transformer to the primary. Connect this pin to GND if not used.
COMP	14	This pin is the transconductance error amplifier output and is made available for loop compensation and optical feedback applications.
VFB	15	This is the inverting input of the error amplifier. It is normally connected to the switching power supply output through a resistor divider. This is the negative input of a transconductance amplifier whose positive input is connected to a reference voltage 1V \pm 3%. Connect this pin to GND if the error amplifier is not used.
DC_ADJ	16	Duty cycle adjust pin. Connect a resistor between this pin and GND to increase the maximum duty cycle.

Pin Name	Pin Number	Pin Description
ROSC	17	Timing resistor connection pin for oscillator frequency programming.
SYNC*	18	Synchronization input pin. Apply an external clock signal for synchronization. Connect this pin to GND if external synchronization is not used. A synchronization after start-up is possible.
CLK*	19	This is the oscillator clock output pin (open drain). It provides a phase-shifted internal clock signal which can be used to synchronize external circuitry.
GD_GND	20	Gate Driver Ground; shall be connected to ground reference.
NC	21	Not connected pins; shall be grounded to a reference voltage.
Chassis	22	Connection to the hybrid metallic chassis

Table 1: Pin function

Electrical characteristics and settings

Parameter	Symbol	Maximum Rating
Supply Voltage	PVIN	120V
Auxiliary Voltage – Gate driver Voltage	AUX	20V
MOSFET Drain-Source	V _{D-S-XXHFC60} V _{D-S-XXHFC100}	150V 250V
Synchronization Signal	SYNC	40V
Clock signal	CLK	40V
Enable	EN	40V
AUX Over Voltage protection adjustment pin	OV_ADJ	40V
Input of the current sense signal	I_SENSE	40V
Duty cycle Adjustment Pin	DC_ADJ	3.6V
Switching frequency Adjustment Pin	ROSC	3.6V
Negative input of the Error Amplifier	VFB	3.6V
Magnetic feedback pulsed current PIN	MFB	3.6V
Error Status	ERROR	40V
Junction Temperature	T _j	150°C

Table 2: Absolute Maximum Rating

Parameter	Symbol	Description															
Oscillation frequency Adjustment	ROSC	The switching frequency is set according to the following equation: $f_{switch} = \frac{10k\Omega}{R_{osc}} \times 1MHz$															
Duty Cycle Adjustment	DC_ADJ	The maximum duty cycle is set according to the following equation: $DC_{max} = 1 - \frac{30.1k\Omega / R_{DC_ADJ}}{30.1k\Omega + (30.1k\Omega / R_{DC_ADJ})}$															
Magnetic Feedback auxiliary pulsed current	MFB	Pulsed current starting at beginning of the minimum off time; current is $\geq 1mA$. The current source slew rate is $>1mA/ns$. The MFB current pulse on time should be 10% of the PWM period. During the MFB current pulse off-time the MFB pin is high-ohmic ($>2k\Omega$) between 0V and this negative clamping voltage ($\geq 0.3V$), to allow demagnetisation of the feedback transformer.															
Synchronization	SYNC	Input pad for synchronization to an external frequency (to the falling edge). A synchronisation clock can be applied in running condition. The synchronization frequency shall be $\pm 10\%$ of the frequency set at ROSC pin.															
Enable	EN	Enable input pad: The EN pad is a digital input that enables or disables the regulator. Set the EN pad high to turn the regulator on; set it to ground, to turn the regulator off. The EN pad includes an internal pull-up. An OFF/ON sequence will reset the AUX Over Voltage latching protection.															
Error amplifier	VFB, COMP	The COMP interface of the transconductance error amplifier is used for loop compensation. VFB is the negative input of the error amplifier. The positive input is connected to a reference voltage of $1V \pm 3\%$. The error amplifier is deactivated if VFB voltage is $>1V$. The transconductance error amplifier offset voltage should be less than $\pm 2mV$. The transconductance error amplifier typical transconductance is $1mA/V$. The transconductance error amplifier gain-bandwidth product should be $>16MHz$. The transconductance error amplifier typical output current is $100\mu A$.															
AUX Over Voltage Protection Adjustment	OV_ADJ	Pin used to adjust the AUX over voltage latching protection, according to the following equations (R_{OV_ADJ} at 0.1%): a) R_{OV_ADJ} connected to ground: $V_{AUX-Th} = 1 + \frac{100k\Omega}{75k\Omega // R_{OV_ADJ}} \pm 3\%$ b) R_{OV_ADJ} connected to AUX: $V_{AUX-Th} = 1 + \frac{100k\Omega // R_{OV_ADJ}}{75k\Omega} \pm 3\%$															
Internal Input Over Voltage protection	INPUT OVP	<table border="1"> <thead> <tr> <th></th> <th>OFF Th Min</th> <th>OFF Th Max</th> <th>ON Th Min</th> <th>ON Th Max</th> </tr> </thead> <tbody> <tr> <td>XXHFC60</td> <td>69.90V</td> <td>74.30V</td> <td>68.50V</td> <td>72.80V</td> </tr> <tr> <td>XXHFC100</td> <td>112.40V</td> <td>119.40V</td> <td>110.10V</td> <td>117.10V</td> </tr> </tbody> </table> <p>The ON and OFF threshold drifts are on the same direction; ON threshold is always $<$ of the OFF Threshold.</p>		OFF Th Min	OFF Th Max	ON Th Min	ON Th Max	XXHFC60	69.90V	74.30V	68.50V	72.80V	XXHFC100	112.40V	119.40V	110.10V	117.10V
	OFF Th Min	OFF Th Max	ON Th Min	ON Th Max													
XXHFC60	69.90V	74.30V	68.50V	72.80V													
XXHFC100	112.40V	119.40V	110.10V	117.10V													

Internal Input Undervoltage Protection	INPUT UVP	<table border="1"> <tr> <th></th> <th>OFF Th Min</th> <th>OFF Th Max</th> <th>ON Th Min</th> <th>ON Th Max</th> </tr> <tr> <td>XXHFC60</td> <td>17.40V</td> <td>18.52V</td> <td>17.75V</td> <td>18.90V</td> </tr> <tr> <td>XXHFC100</td> <td>44.97V</td> <td>47.75V</td> <td>45.80V</td> <td>48.71V</td> </tr> </table>		OFF Th Min	OFF Th Max	ON Th Min	ON Th Max	XXHFC60	17.40V	18.52V	17.75V	18.90V	XXHFC100	44.97V	47.75V	45.80V	48.71V
			OFF Th Min	OFF Th Max	ON Th Min	ON Th Max											
XXHFC60	17.40V	18.52V	17.75V	18.90V													
XXHFC100	44.97V	47.75V	45.80V	48.71V													
The ON and OFF threshold drifts are on the same direction; ON threshold is always > of the OFF Threshold.																	
Internal Output Over-power Protection	I_SENSE limit	The switching is prevented when the I_SENSE input is reaching 1V, limiting the maximum power output that the DC/DC controller can provide.															
Thermal resistance Junction -Case	Rthj-c	9.1°C/W															

Table 3: DC/DC controller characteristics

Ordering Information

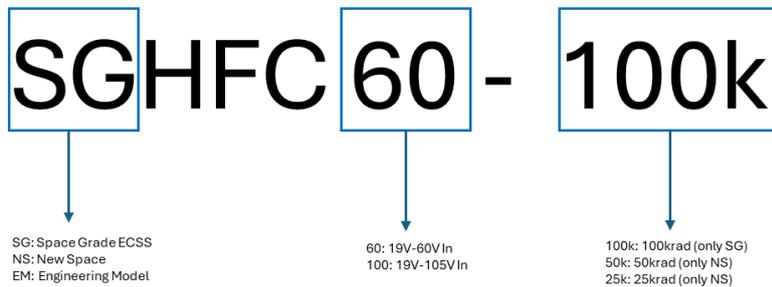


Figure 4: Part number definition

Code Quality Level	Quality Level	Description
SG	Space Grade	Assembly processes ECSS compliant; components ESCC grade 1, JANS, JANTXV; TID 100krad test at component level on batch used for the production. Hybrid Screening and Lot Acceptance test according to ECSS-ST-60-05C.
NS	New Space	IPC Class 3 assembly processes. Components not individually screened or procured according to automotive specification. Customized screening and lot acceptance testing suitable for new space programs performed at hybrid level. Components batches not TID tested if the technology has proven TID performances with at least 100% margin on the program TID requirements. Available 25krad and 50krad options.
EM	Engineering Model	Mechanical and electrical equivalent to the other quality levels but not screened at component or DC/DC module level. Assembled with industrial standard. Recommended for early prototyping.

Figure 5: Quality level codes

Commercial Part Number	Input Bus	TID (Krad)	Level
SGHFC60-100k	19V-60V	100	Space Grade
SGHFC100-100k	50V-105V	100	Space Grade
EMHFC60-100k	19V-60V	-	Engineering Model
EMHFC100-100k	50V-105V	-	Engineering Model
NSHFC60-50k	19V-60V	50	New Space
NSHFC100-50k	50V-105V	50	New Space
NSHFC60-25k	19V-60V	25	New Space
NSHFC100-25k	50V-105V	25	New Space

Table 4: Available DC/DC converter controllers